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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,007	04/18/2001	Mou-Shiung Lin	MEG 01-004	7677

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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	09/837,007	LIN ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *55 and 57-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *55 and 57-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

The terminal disclaimer filed 5/25/07 has been disapproved because there is no common ownership or even common inventor between the patent and the present application. Please note that a terminal disclaimer for this patent was not required in the previous office action. The double patenting rejections previous written and re-written below, are over other applications and therefore are provisional double patenting rejections. Terminal disclaimers are not required until one is patented.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In *re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 55,57-65 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 53, 58, 59 and 67 of copending Application No. 10/935,451 in view of Yoneda et al., US Patent 6,229,711.

This is a provisional obviousness-type double patenting rejection.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the combination of claims 53 and 67 of the other application combine to teach all of the limitations of the present claim 55, except for the limitation reciting a substrate comprising a first pad with a sidewall not covered by a solder mask.

Yoneda teaches the substrate [12] comprises a first pad [20] with a sidewall not covered by a solder mask (figure 5A).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the first pad with a sidewall not covered by a solder mask of Yoneda in the invention of Ohuchi because Yoneda teaches the insulating layer [sic:solder layer] from spreading (3, 51+) and protects the remaining parts (5, 7+).

The remaining claims correspond as follows:

Present Application	10/935,451
56	intended use/US Patent 5,075,965
57	68
58	59
59	58

Regarding claims 60 and 61, while 10/935,451 fails to teach said substrate comprises a ball grid array (BGA) substrate, it would have been obvious to one of

ordinary skill in the art at the time of the invention to use a BGA substrate as the substrate in the invention of 10/935,451 because BGA substrates are conventionally known substrates to which chip packages are attached. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07). A skilled artisan would use a BGA substrate in order to allow for integration of the chip package into a system, such as a computer.

With respect to claim 61, while 10/935,451 fails to teach a contact ball under said substrate, wherein said semiconductor device is over said substrate, a contact ball under the substrate with a chip on the other side describes a BGA substrate, as taught above in claim 60.

As to claims 62 and 63, while 10/935,451 fails to teach an underfill (claim 62) or molding compound (claim 63) between said semiconductor device and said substrate, the use of an underfill or molding compound is conventionally known to skilled artisans in order to protect the electrical connection form contaminants, such as moisture. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

In re claim 64, Yoneda teaches said substrate further comprises a second pad neighboring to said first pad and having an edge not covered by a solder mask, and wherein no solder mask traverses between said first and second pads (figure 5).

Regarding claim 65, while 10/935,451 fails to teach said first region is coplanar with said second region, a skilled artisan could reasonably state that it is "substantially"

coplanar because the specification doesn't positively recite a definition or range for "substantially". Therefore, even though 10/935,451 fails to teach substantially" coplanar, one could say that this is "substantially" coplanar since the term isn't defined in the specification (MPEP 2173.05(b)D).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 55-59 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-10 of copending Application No. 11/389,717. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-3 and 5 of the copending application combine to meet the limitations of claim 1 of the present application.

The remaining claims correspond as follows:

Present Application	11/389,717
56	1
57	6
58	8
59	4

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Regarding claims 60 and 61, while Ohuchi and Yoneda fail to teach said substrate comprises a ball grid array (BGA) substrate, it would have been obvious to

one of ordinary skill in the art at the time of the invention to use a BGA substrate as the substrate in the invention of Ohuchi because BGA substrates are conventionally known substrates to which chip packages are attached. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07). A skilled artisan would use a BGA substrate in order to allow for integration of the chip package into a system, such as a computer.

With respect to claim 61, while Ohuchi fails to teach a contact ball under said substrate, wherein said semiconductor device is over said substrate, a contact ball under the substrate with a chip on the other side describes a BGA substrate, as taught above in claim 60.

As to claims 62 and 63, while Ohuchi fails to teach an underfill (claim 62) or molding compound (claim 63) between said semiconductor device and said substrate, the use of an underfill or molding compound is conventionally known to skilled artisans in order to protect the electrical connection form contaminants, such as moisture. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

In re claim 64, Yoneda teaches said substrate further comprises a second pad neighboring to said first pad and having an edge not covered by a solder mask, and wherein no solder mask traverses between said first and second pads (figure 5).

Regarding claim 65, while Ohuchi fails to teach said first region is coplanar with said second region, a skilled artisan could reasonably state that it is "substantially"

coplanar because the specification doesn't positively recite a definition or range for "substantially". Therefore, even though Ohuchi teaches an overlap, one could say that this is "substantially" coplanar since the term isn't defined in the specification (MPEP 2173.05(b)D).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 55, 57-65 are rejected under 35 U.S.C. 103(a) as being obvious over Ohuchi et al. US Patent 6,495,916, in view of Yoneda et al., US Patent 6,229,711.

Ohuchi (Figure 7) teaches a chip package, comprising:

a semiconductor device [1];

a substrate (1, 51+);

a metal pillar [4] between said semiconductor device and said substrate, wherein said metal pillar has a thickness of between 10 and 100 microns (3, 1+);

a metal layer [14] between said metal pillar and said substrate, wherein said metal layer has a bottom surface having a first region partially covered by said metal pillar and a second region not covered by said metal pillar; and

a solder metal [7] between said metal layer and said substrate, wherein said solder metal is bonded to said first pad (1, 51+, while not specifically taught, the substrate inherently has to have a pad to which the solder metal can electrically connect).

Ohuchi fails to teach the substrate comprises a first pad with a sidewall not covered by a solder mask.

Yoneda teaches the substrate [12] comprises a first pad [20] with a sidewall not covered by a solder mask (figure 5A).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the first pad with a sidewall not covered by a solder mask of Yoneda in the invention of Ohuchi because Yoneda teaches the insulating layer [sic:solder layer] from spreading (3, 51+) and protects the remaining parts (5, 7+).

As to claim 57, while Ohuchi fails to teach the distance between an edge of said metal layer and an edge of said metal pillar is greater than 0.2 microns, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize this distance through routine experimentation (MPEP 2144.05).

With respect to claim 58, Ohuchi teaches the semiconductor device comprises a pad [2] and a passivation layer [5], said pad exposed by an opening in said passivation layer, wherein said metal pillar is over said pad.

In re claim 59, while Ohuchi fails to teach a barrier between said bump and said pad, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a barrier between a bump and an underlying surface because it improves the adhesion between the two and to keep the solder from diffusing into the underlying material.

Regarding claims 60 and 61, while Ohuchi and Yoneda fail to teach said substrate comprises a ball grid array (BGA) substrate, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a BGA substrate as the substrate in the invention of Ohuchi because BGA substrates are conventionally known substrates to which chip packages are attached. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07). A skilled artisan would use a

BGA substrate in order to allow for integration of the chip package into a system, such as a computer.

With respect to claim 61, while Ohuchi fails to teach a contact ball under said substrate, wherein said semiconductor device is over said substrate, a contact ball under the substrate with a chip on the other side describes a BGA substrate, as taught above in claim 60.

As to claims 62 and 63, while Ohuchi fails to teach an underfill (claim 62) or molding compound (claim 63) between said semiconductor device and said substrate, the use of an underfill or molding compound is conventionally known to skilled artisans in order to protect the electrical connection form contaminants, such as moisture. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

In re claim 64, Yoneda teaches said substrate further comprises a second pad neighboring to said first pad and having an edge not covered by a solder mask, and wherein no solder mask traverses between said first and second pads (figure 5).

Regarding claim 65, while Ohuchi fails to teach said first region is coplanar with said second region, a skilled artisan could reasonably state that it is "substantially" coplanar because the specification doesn't positively recite a definition or range for "substantially". Therefore, even though Ohuchi teaches an overlap, one could say that this is "substantially" coplanar since the term isn't defined in the specification (MPEP 2173.05(b)D).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication from the examiner should be directed to David A. Zarneke at (571)-272-1937. If attempts to reach the examiner are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number where this application is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David A. Zarneke/
Primary Examiner
8/8/07